REMARKS

Status of the Claims

Claims 38-47 and 49-55 are pending, with Claims 38, 40, 42, 44, and 45 being independent. Claims 53-55 have been added and Claims 38, 44, and 45 have been amended. Specifically, Claims 38, 44, and 45 have been amended to clarify that the spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer are formed "by depositing a film selected from the group consisting of phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then anisotropic etching the film." Support for the amendments and new claims may be found in the specification as originally filed, for example, at page 8, lines 10-17. No new matter has been added.

Initially, Applicant would like to thank the Examiner for indicating that Claims 40-43 are allowed.

Applicant respectfully requests the Examiner to reconsider and withdraw the outstanding rejections in view of the foregoing amendments and following remarks.

Claim Rejections Under 35 U.S.C. § 103(a)

Claims 38, 39, 44-47, and 49-52 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,200,352 ("Pfiester") in view of U.S. Patent No. 5,880,508 ("Wu") in further view of alleged admitted prior art ("alleged APA") or U.S. Patent No. 4,947,081 ("Ohiwa").[1] This rejection is respectfully traversed.

Amended independent Claims 38, 44, and 45 each recite a method for fabricating a MOS device having a gate width of less than 0.3 micron comprising a combination of features that includes forming spacers adjacent to a gate electrode and on an upper surface of a high dielectric constant layer *by depositing a film selected from the group consisting of phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then anisotropic etching the film.* Claims 39, 46, 47, 50, and 53 are dependent upon independent Claim 38, Claims 51 and 54 are dependent upon independent Claim 44, and Claims 49, 52, and 55 are dependent upon independent Claim 45.

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[1] 1. Pfeister is cited as allegedly disclosing, *inter alia*, "forming an interfacial layer (14, fig. 1A), comprising silicon nitride or silicon oxynitride, on a silicon semiconductor substrate" and "forming spacer (20, fig. 1A) adjacent to the gate electrode and on an upper surface of the interfacial layer (col. 5, lns. 30-41)." (Official Action at page 2). Applicant respectfully submits that Pfeister does not disclose forming an interfacial layer comprising either silicon nitride or silicon oxynitride. Rather, Pfeister discloses that the dielectric layer "is usually a thermally grown, dry silicon dioxide, but can be oxide-nitride-oxide (ONO) or a similar dielectric material." (Column 2, Lines 53-55 of Pfeister).

2. Wu is cited as allegedly disclosing, *inter alia*, "forming a high dielectric constant layer (8, fig. 1) on the interfacial layer (6, fig. 1), the [sic] comprises a material that is selected from the group consisting of Ta_2O_5, wherein the interfacial layer comprises silicon nitride or silicon oxynitride." It is not seen where the alleged disclosure of a silicon nitride interfacial layer is found in Wu. As such, the Examiner is requested to identify the portion of Wu considered to disclose a silicon nitride interfacial layer.

3. The Examiner is requested to cite specific portions of any prior art references encompassed by the alleged APA and explain where any such prior art provides the requisite motivation or incentive to

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP § 2143.

Applicant respectfully submits that the combination of Pfeister, Wu, non-analogous Ohiwa[2], and alleged APA fails to suggest the combination of steps recited in amended independent Claims 38, 44, and 45, which includes forming source and drain regions in the substrate adjacent to the gate electrode and forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer by depositing a film selected from the group consisting of phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then anisotropic etching the film.

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modify Pfiester in view of Wu in a manner which would result in the various combinations of features recited in independent Claims 38, 44, and 45.

[2] The Official Action acknowledges that Pfeister and Wu fail to disclose a high dielectric layer comprising $Ta_2(O_{1-x}N_x)_5$. Accordingly, the alleged APA on page 6, lines 24-26 of the present specification and Ohiwa are cited as allegedly disclosing that a high dielectric layer can be formed of $Ta_2(O_{1-x}N_x)_5$. (Official Action at page 2).

"In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). MPEP § 2141.01(a).

Applicant respectfully submits that Ohiwa, related to a thin film electroluminescence device, is nonanalogous art to the transistor of Pfiester or Wu. Applicant further respectfully submits that Ohiwa is not reasonably pertinent to the particular problem with which the inventor was concerned, methods for fabricating integrated circuits using metal oxide semiconductor (MOS) technology. (Page 1, Lines 4-5). As such, Ohiwa may not be relied upon as a basis for rejection of the presently claimed methods.

Pfeister discloses a dielectric layer 14, usually a thermally grown, dry silicon dioxide, but can be oxide-nitride-oxide (ONO) or a similar dielectric material, formed overlying a substrate 12 made from any semiconductive material. (Column 2, Lines 49-55 of Pfeister). An insulated conductive control region or gate 16, usually made of polysilicon or a similar conductive material, is formed overlying the dielectric layer 14. (Column 2, Lines 55-58 of Pfeister). A dielectric region 18, which can be nitride, silicon dioxide (SiO_2), tetra-ethyl-ortho-silicate (TEOS), boro-phosphate-silicate-glass (BPSG), or a similar dielectric, is formed overlying the gate 16. (Column 2, Lines 58-62 of Pfeister). The gate 16 is reoxidized to form dielectric regions 20, which protect the gate 16 and ensure that the gate 16 is electrically isolated. (Column 2, Lines 62-65 of Pfeister). A first spacer 22, usually made from a dielectric material, is formed overlying the dielectric layer 14 and adjacent to the dielectric regions 18 and 20. (Column 2, Line 66 – Column 3, Line 1 of Pfeister).

Subsequently, a Doping step, usually an ion implantation process, is performed which creates a first doped region and a second doped region, referred to as lightly doped drain regions or LDD regions 28, adjacent to epitaxial regions 24 and underlying dielectric layer 14. (Column 3, Lines 36-42 of Pfeister). Subsequent processing, such as overlying conductive layer formation and heat cycles, drives the doping of the epitaxial regions into the substrate to form source and drain regions 32, which underlie the epitaxial regions 24 and respectively electrically contact to the LDD regions 28 that are adjacent to the epitaxial regions 24. (Column 4, Lines 10-16 of Pfeister).

I. **Claims 38, 39, 45-47, 49, 50, 52, 53, and 55**

Applicant respectfully submits that the combination of Pfeister, Wu, non-analogous Ohiwa, and alleged APA does not disclose or suggest all the claim limitations of independent Claims 38 and 45, for Pfeister does not disclose or suggest forming source and drain regions in the substrate adjacent to the gate electrode and forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer by depositing a film selected from the group consisting of phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then anisotropic etching the film, as recited in independent Claims 38 and 45. Rather, Pfeister discloses reoxidizing a gate 16 to form dielectric regions 20, forming a first spacer 22 overlying the dielectric layer 14 and adjacent to the dielectric regions 18 and 20, and subsequently creating lightly doped drain regions 28 and forming source and drain regions 32. None of Wu, non-analogous Ohiwa, or alleged APA cures the deficiencies of Pfeister in this regard.

Applicant further respectfully submits that the Official Action fails to explain why a person of ordinary skill would have been motivated to combine the tantalum oxynitride layer provided between a first insulation layer and a transparent electrode of non-analogous Ohiwa with the dielectric layer of Wu to provide the presently claimed high dielectric constant layer comprising $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6.

Accordingly, for at least the above-noted reasons, Applicant respectfully submits that the Official Action has not set forth a *prima facie* case of obviousness. Accordingly, withdrawal of the rejection is respectfully requested.

II. **Claims 44, 51, and 54**

Both Pfeister and Wu fail to disclose a transistor having a silicon nitride interfacial layer. While the Official Action asserts that Pfeister discloses "forming an interfacial layer (14, fig. 1A), comprising silicon nitride or silicon oxynitride, on a silicon semiconductor substrate," and that Wu discloses "forming a high dielectric constant layer (8, fig. 1) on the interfacial layer (6, fig. 1), the comprises [sic] a material that is selected from the group consisting of Ta_2O_5, wherein the interfacial layer comprises silicon nitride or silicon oxynitride," Applicant points out that Pfeister discloses forming a dielectric layer that is usually a thermally grown, dry silicon dioxide, but can be oxide-nitride-oxide (ONO) or a similar dielectric material, and Wu discloses forming a silicon oxynitride interfacial layer. Specifically, Wu discloses forming a silicon oxynitride layer on the top surface of a single crystal silicon substrate and depositing a thin dielectric layer with high permitivity on the silicon oxynitride layer.

Thus, Applicant respectfully submits that the combination of Pfeister, Wu, non-analogous Ohiwa, and alleged APA does not disclose or suggest all the claim limitations of Claim 44. In particular, neither Pfeister nor Wu discloses or suggests forming a silicon nitride interfacial layer on a semiconductor substrate and, as noted above, Pfeister does not disclose or suggest forming source and drain regions in the substrate adjacent to the gate electrode and forming spacers adjacent to the gate electrode and on an upper surface of the high dielectric constant layer by depositing a film selected from the group consisting of phosphosilicate glass, oxides, and nitrides over the entire surface of the device and then

anisotropic etching the film, as recited in independent Claim 44. None of Wu, non-analogous Ohiwa, or alleged APA cures the deficiencies of Pfeister in this regard.

Accordingly, for at least the above-noted reasons, Applicant respectfully submits that the Official Action has not set forth a *prima facie* case of obviousness. Accordingly, withdrawal of the rejection is respectfully requested.

Conclusion

For the reasons noted above, the art of record does not disclose or suggest the inventive concept of the presently claimed invention as defined by the claims.

In view of the foregoing amendments and remarks, reconsideration of the claims and allowance of the subject application is earnestly solicited. The Examiner is invited to contact the undersigned at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

Respectfully submitted,

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